Relationship of the units

- Basic unit, latch and F/F (unit 11)
- Simple sequential circuits (unit 12)
  - Registers
  - Counters
- Complex sequential circuits : FSM (finite state machine)
  - Simple one: analysis, Mealy & Moore (unit 13)
  - Complex one:
    - Derive state graph and tables (unit 14)
    - Reduce state graph and tables (unit 15)

Unit 12

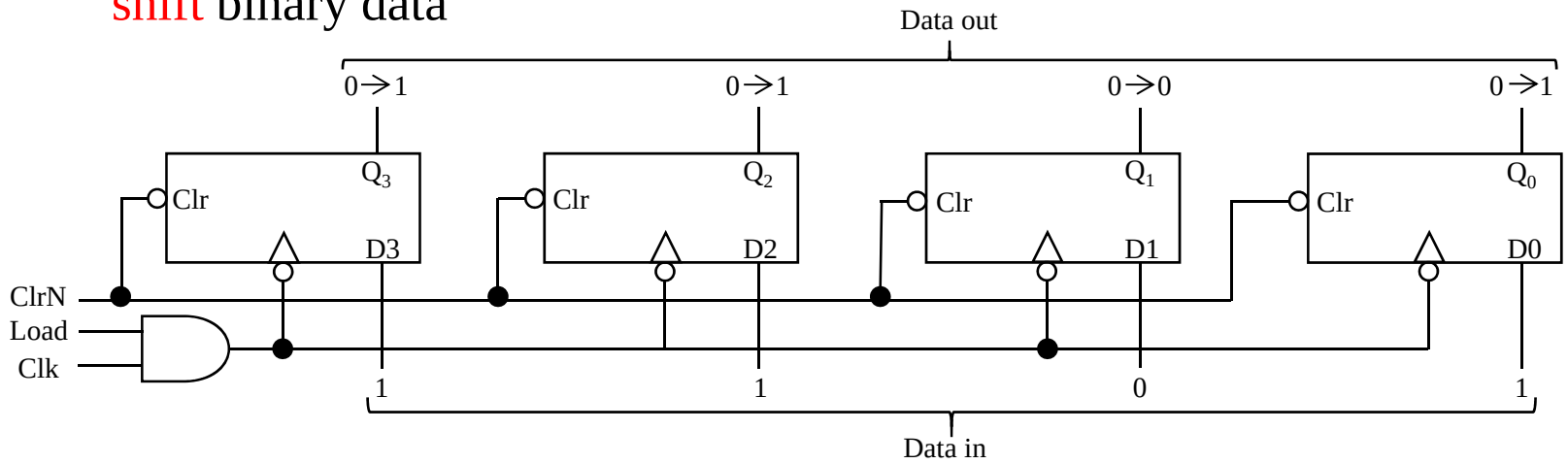
Registers and Counters

Outline

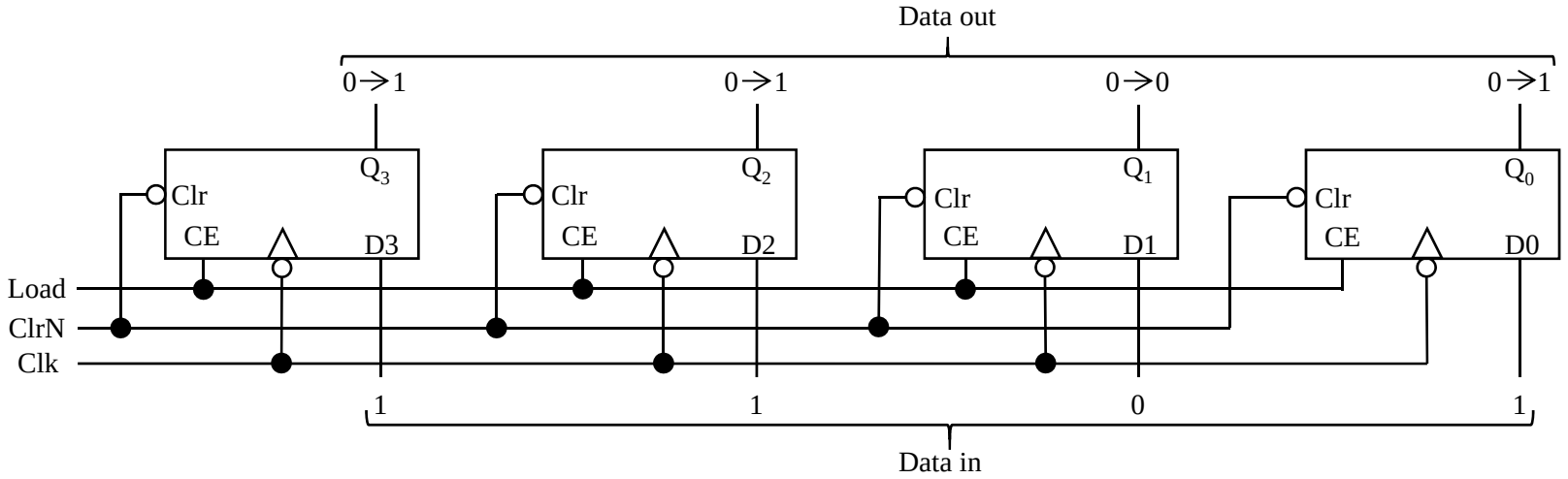
- Registers
  - Operation
  - Application to shift registers
- Counters
  - How to build and how it works
  - Counter application and how to derive the F/F's input equations

Registers and Register Transfer (1/3)

Registers: a group of F/Fs with a common clock input, used to store and shift binary data

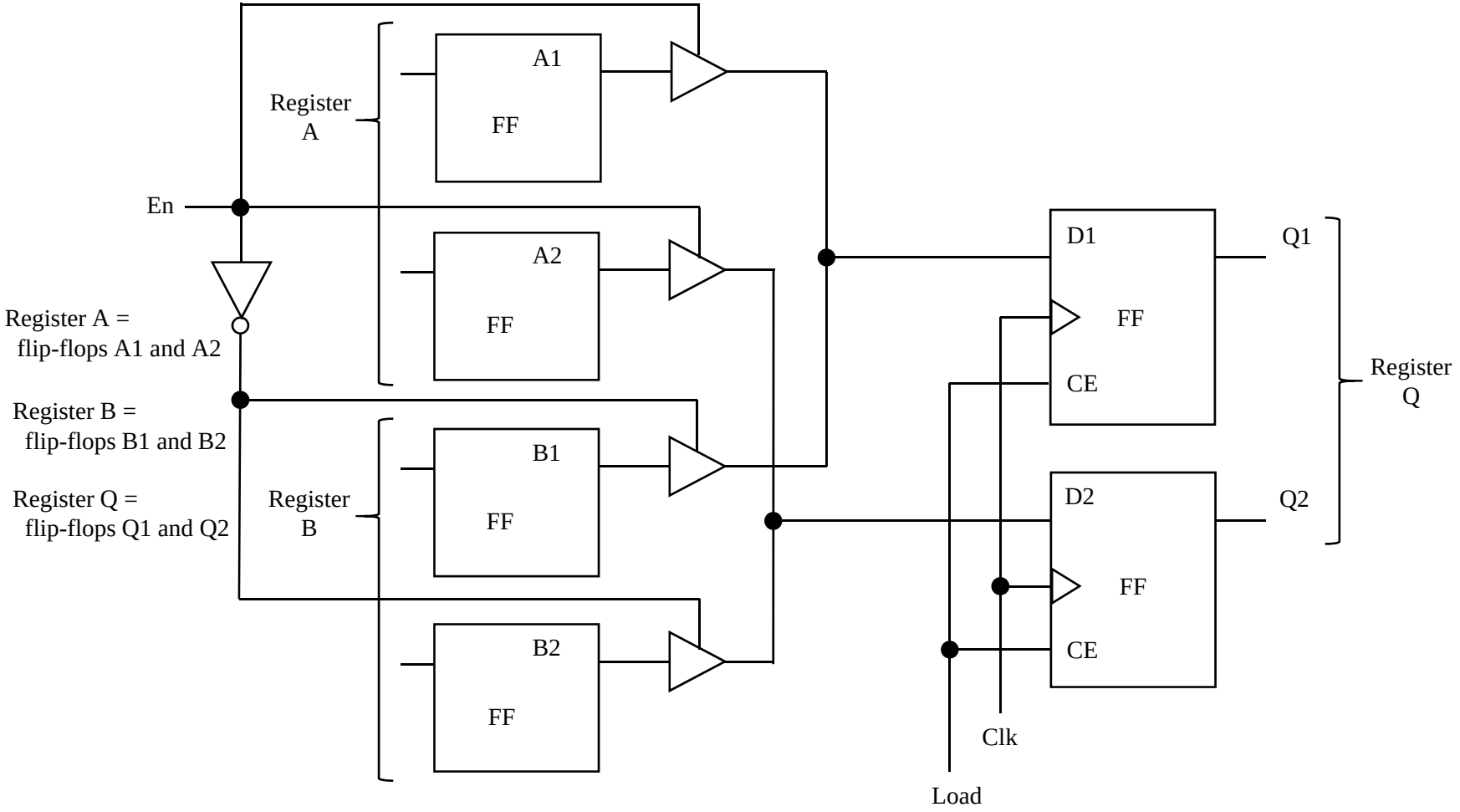


(a) Using gated clock



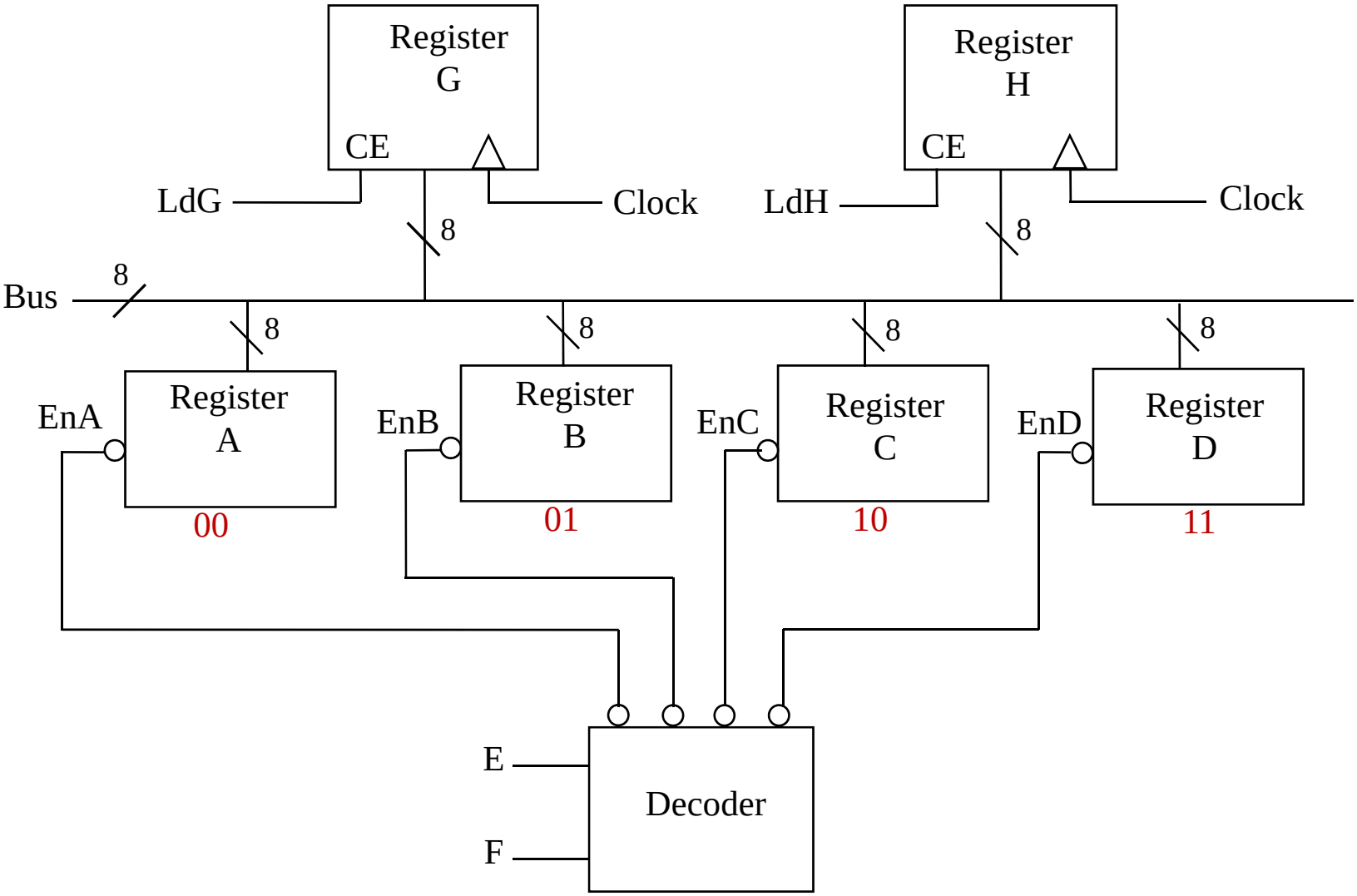
(b) With clock enable

Registers and Register Transfer (2/3)



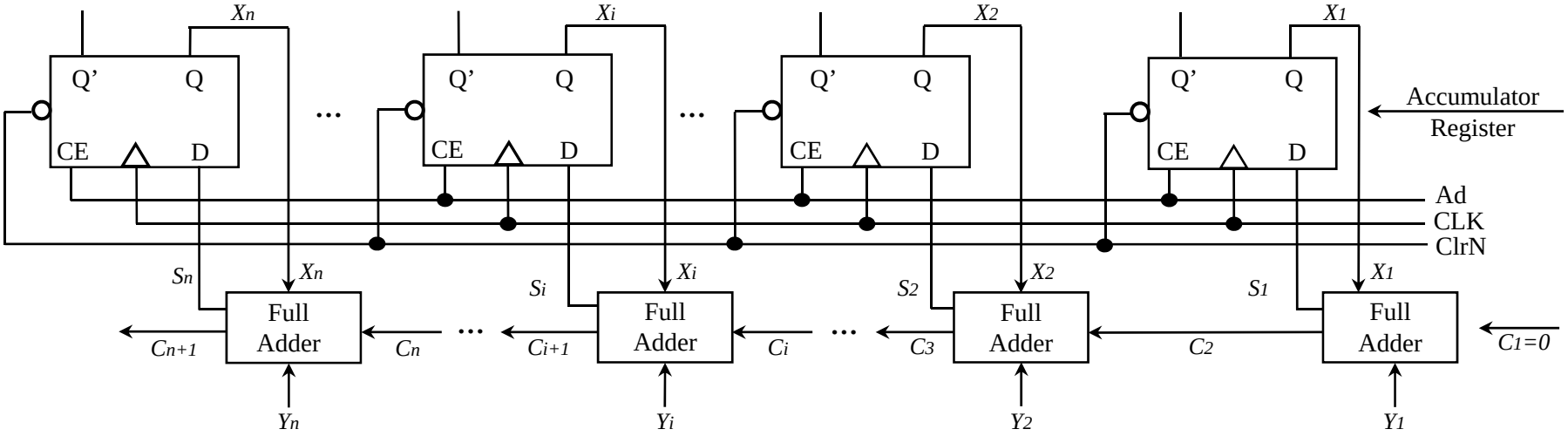
Data transfer between registers, equiv. to 2:1 MUX

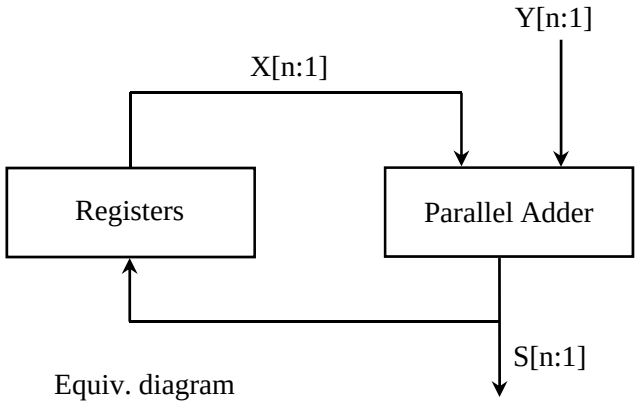
Registers and Register Transfer (3/3)

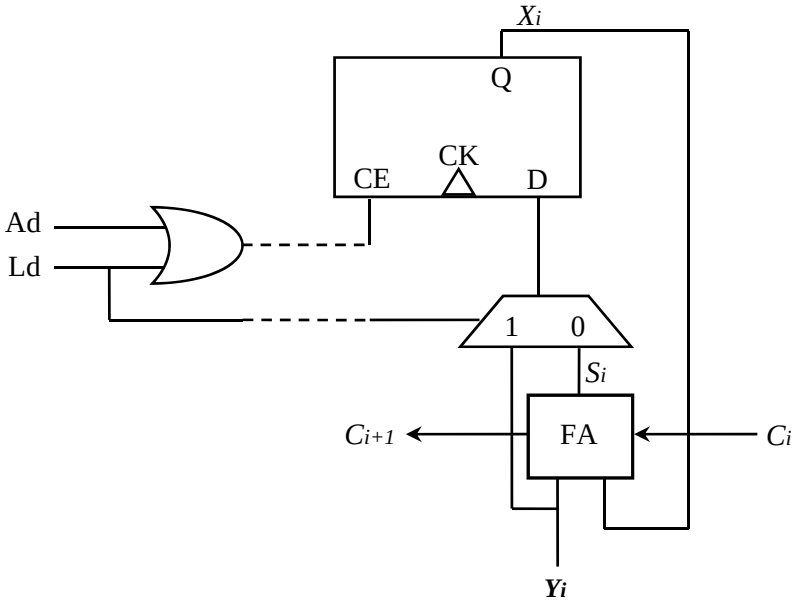


Data transfer using a tri-state bus

Parallel Adder with Accumulator





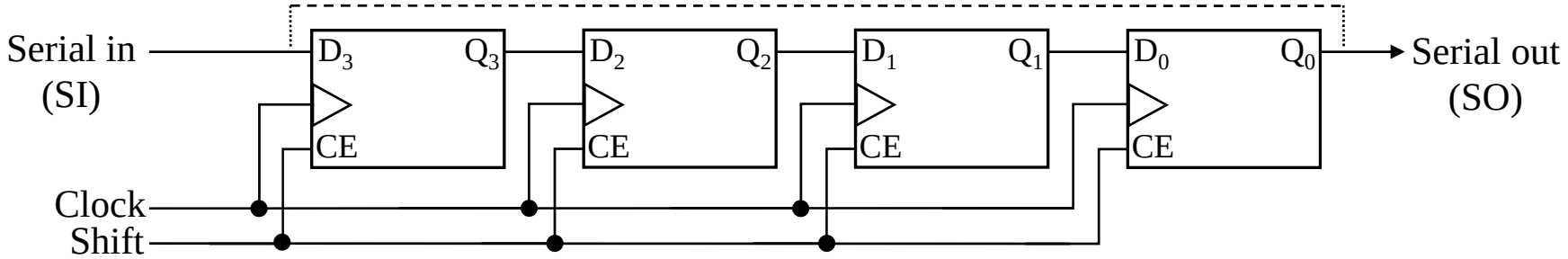


Equiv. diagram

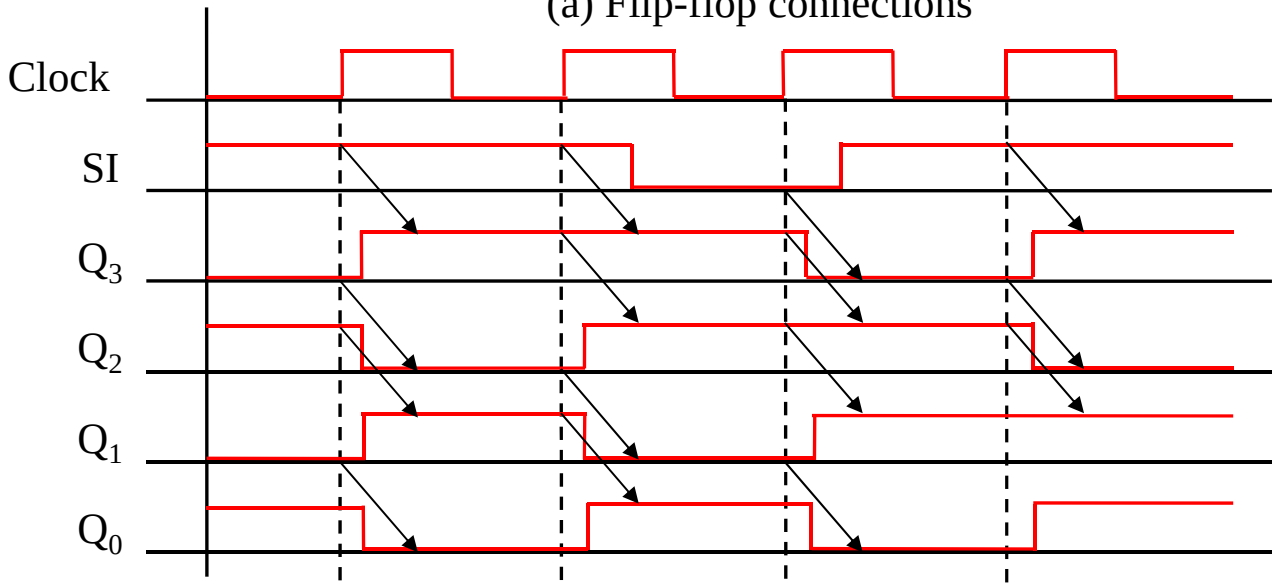
Adder with MUX to load initial value

Shift Registers (1/6)

Shift Registers: a group of F/Fs in which a binary number can be stored. This number can be shifted left or right when a shift signal is applied



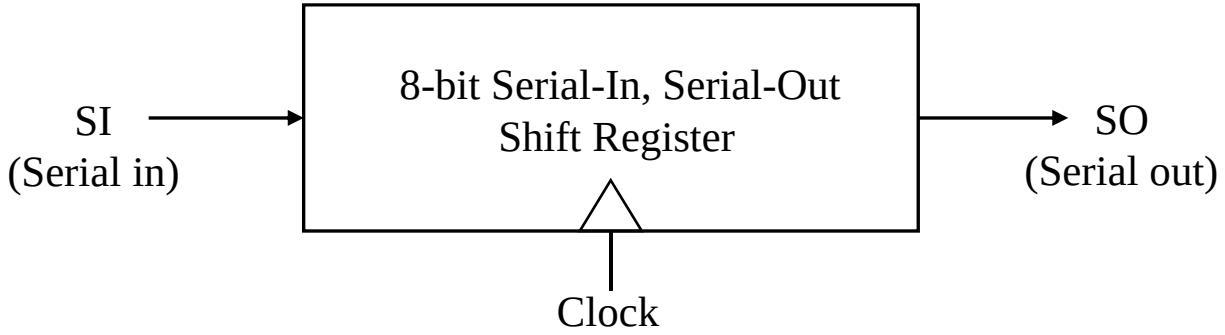
(a) Flip-flop connections



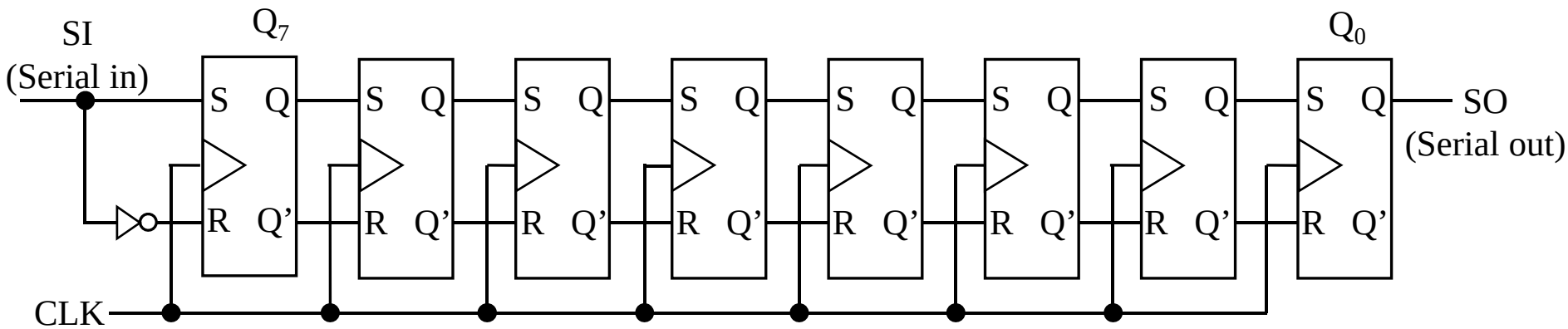
(b) Timing diagram

Shift Registers (2/6)

Serial in, serial out

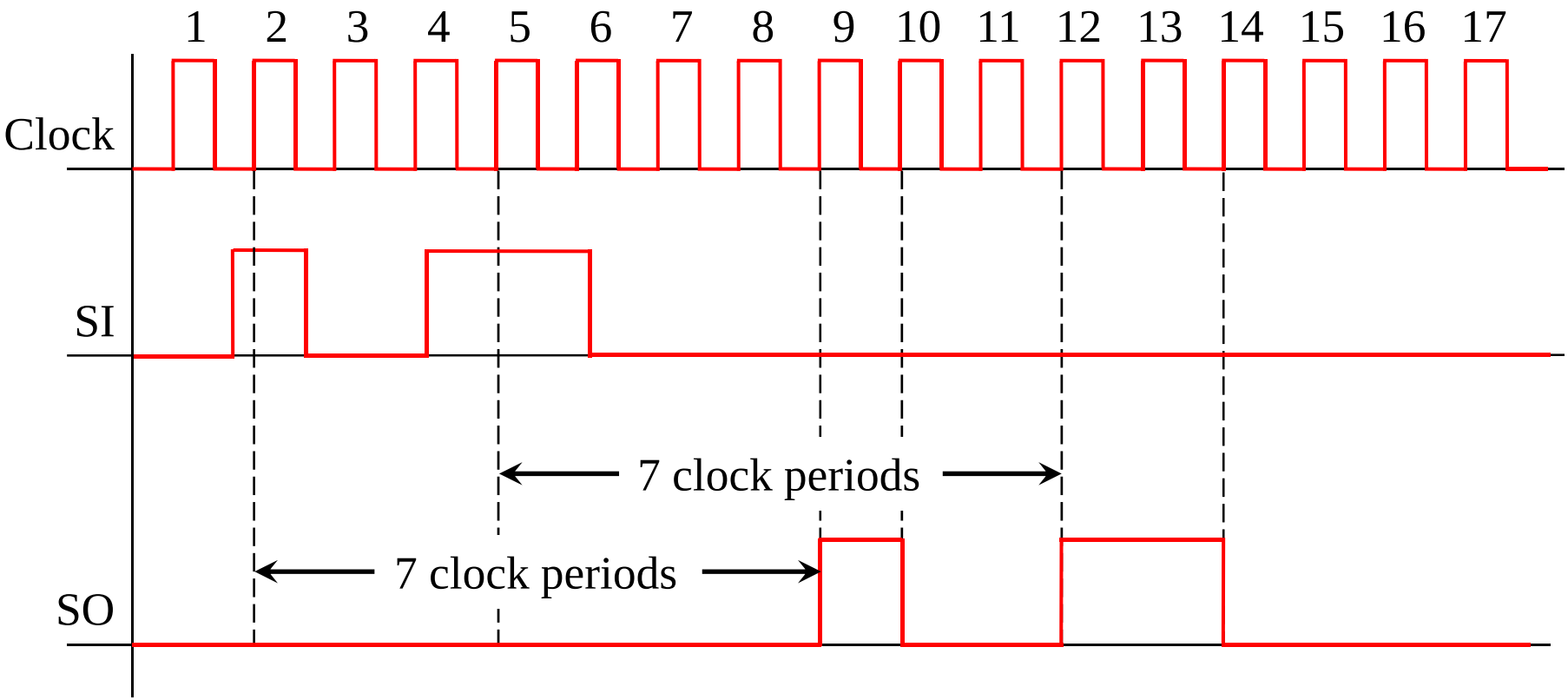


(a) Block diagram



(b) Logic diagram

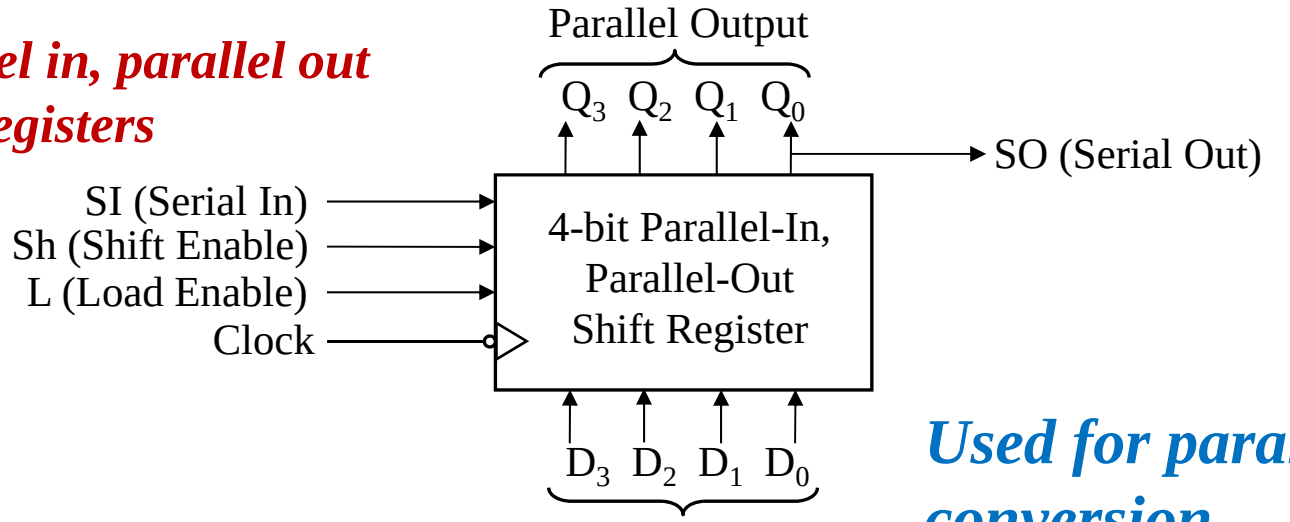
Shift Registers (3/6)



Take (n-1) cycles to output for n-bit shift registers

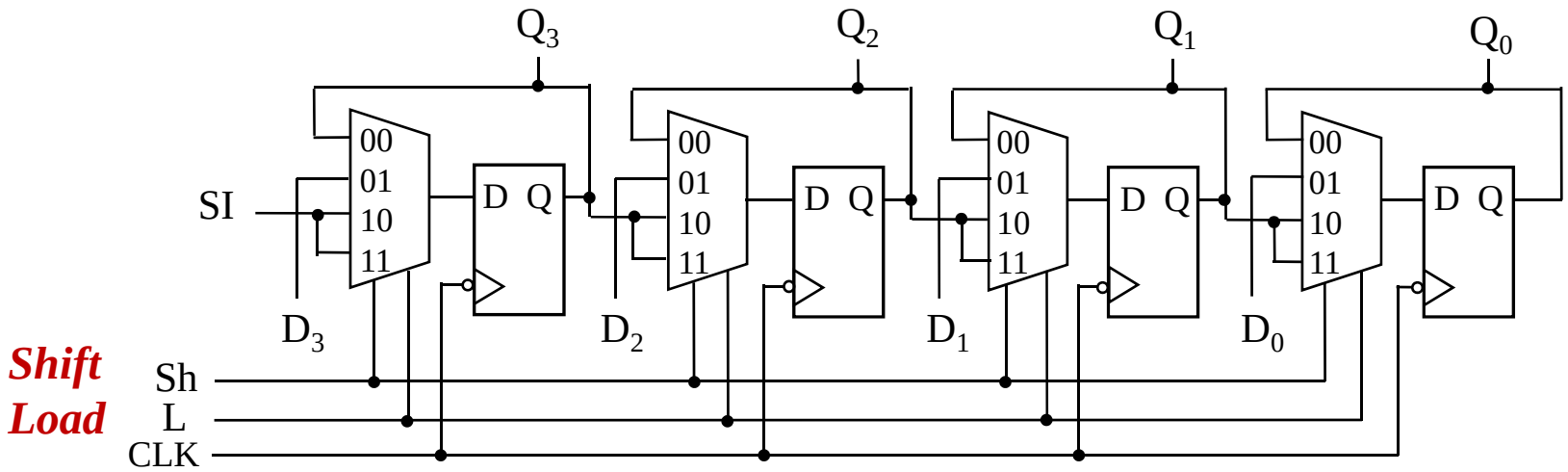
Shift Registers (4/6)

Parallel in, parallel out shift registers



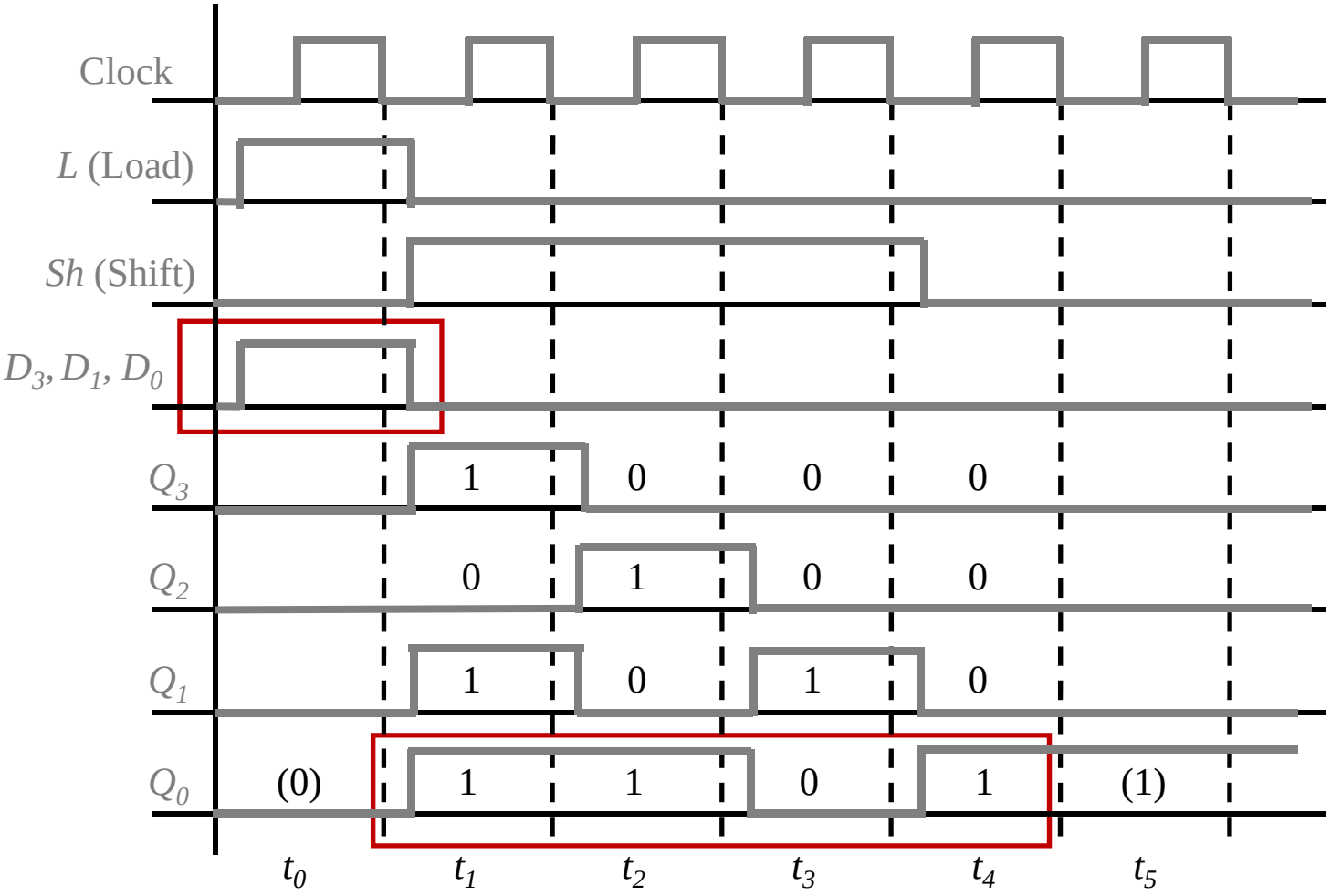
(a) Block diagram

Used for parallel to serial conversion



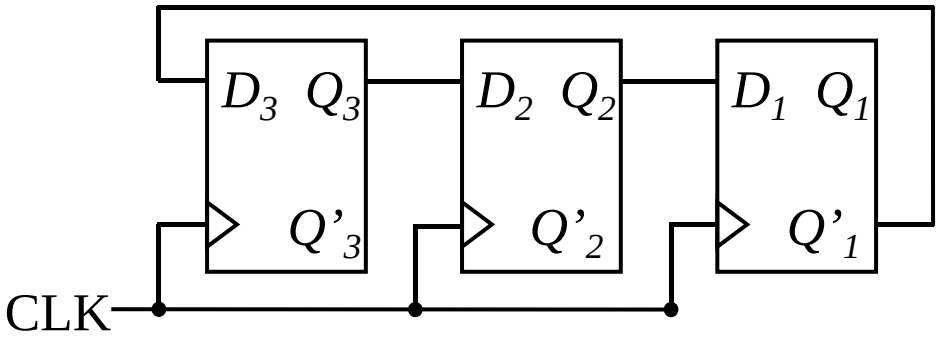
(b) Implementation using flip-flops and MUXes

Shift Registers (5/6)

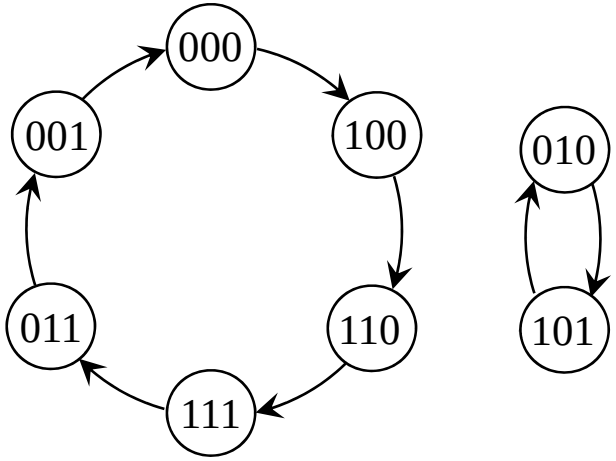


Used for parallel to serial conversion
e.g., convert parallel 1011 to serial 1101

Shift Registers (6/6)



(a) Flip-flop connections



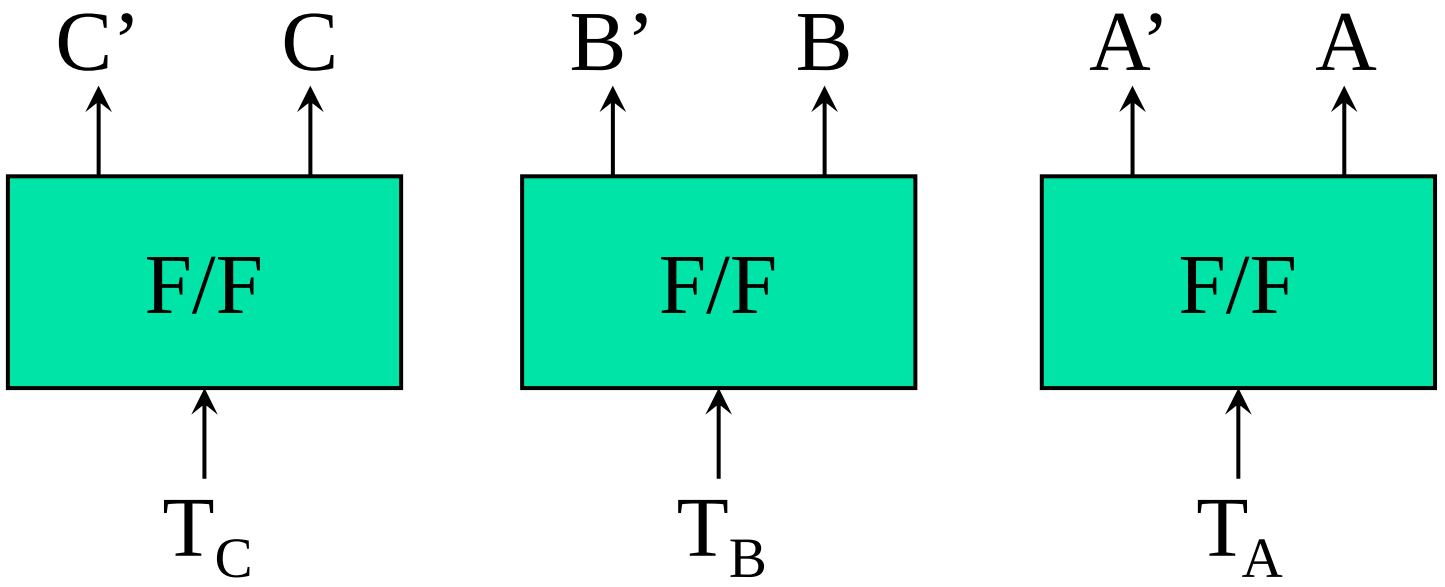
(b) State graph

Counter: circuit that cycles through a fixed sequence of states

Johnson counter: shift register with inverted feedback

Design of a Binary Counter (1/11)

With T F/F



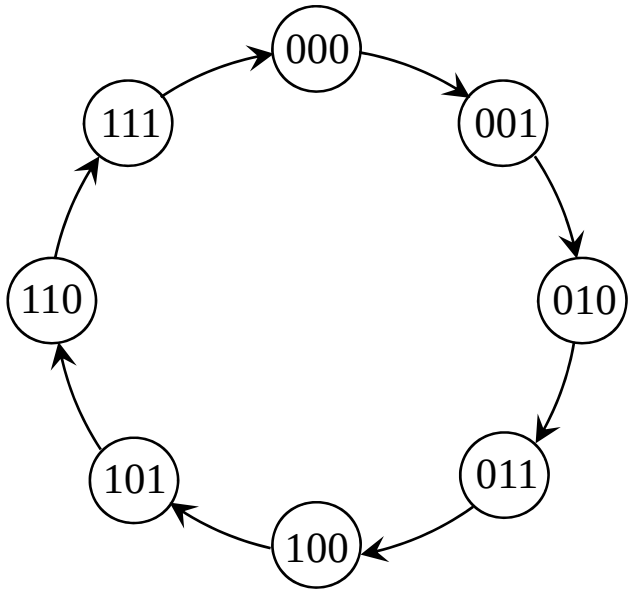
$$CBA : 000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 111$$

Synchronous counter triggered by a clock

Design of a Binary Counter (2/11)

$$CBA : 000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 111$$

State graph

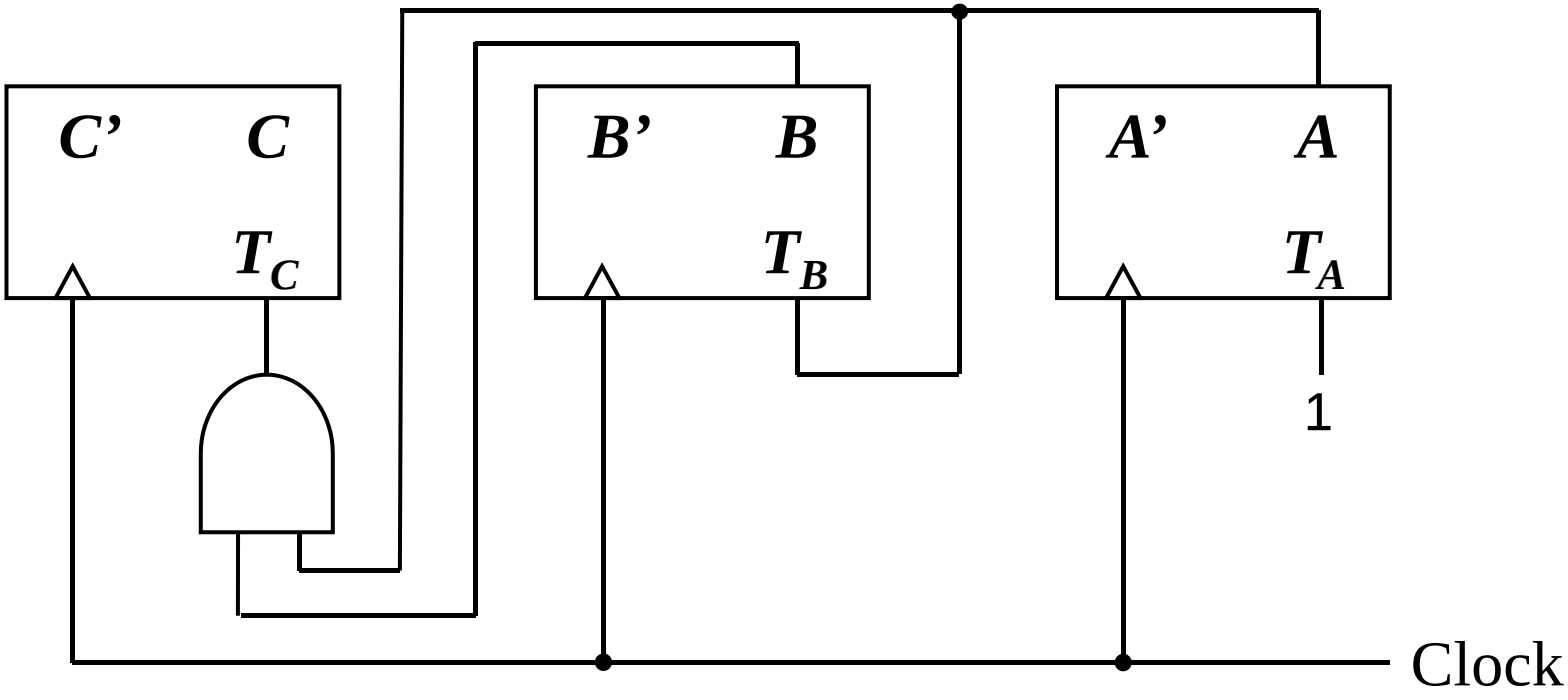


Design of a Binary Counter (3/11)

A changes (counts) as long as T-F/F(A) triggered

B changes (counts) as long as A=1 & T-F/F(B) triggered

C changes (counts) as long as A=B=1 & T-F/F(C) triggered



Design of a Binary Counter (4/11)

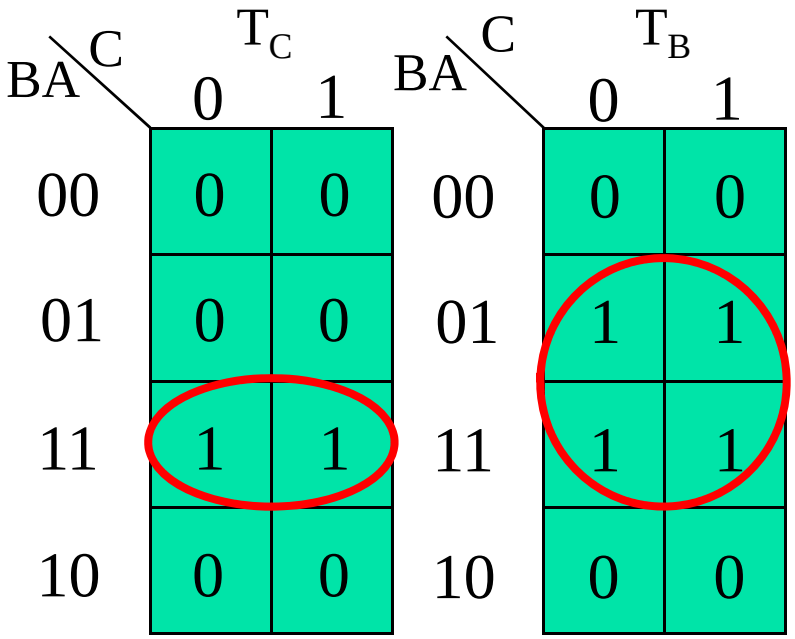
Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Systematic method: state table

Present state Next state F/F inputs

C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Tips: T = 1 iff Q ≠ Q⁺



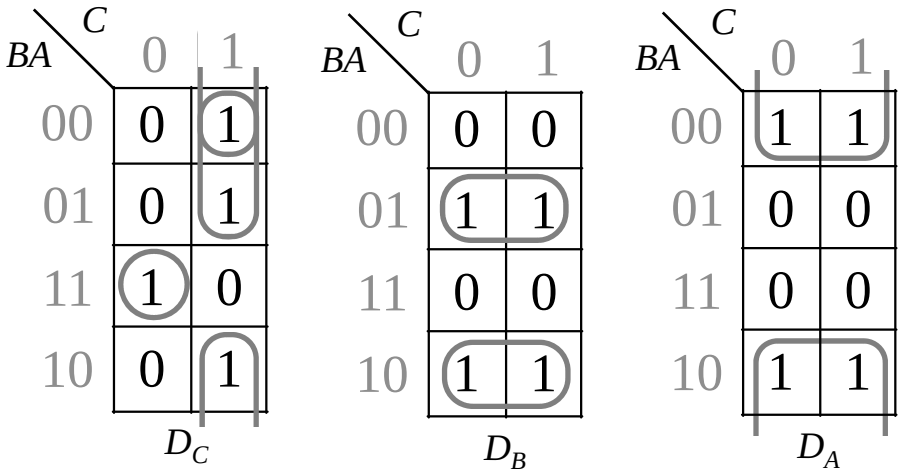
$T_C = BA$ $T_B = A$

Design of a Binary Counter (5/11)

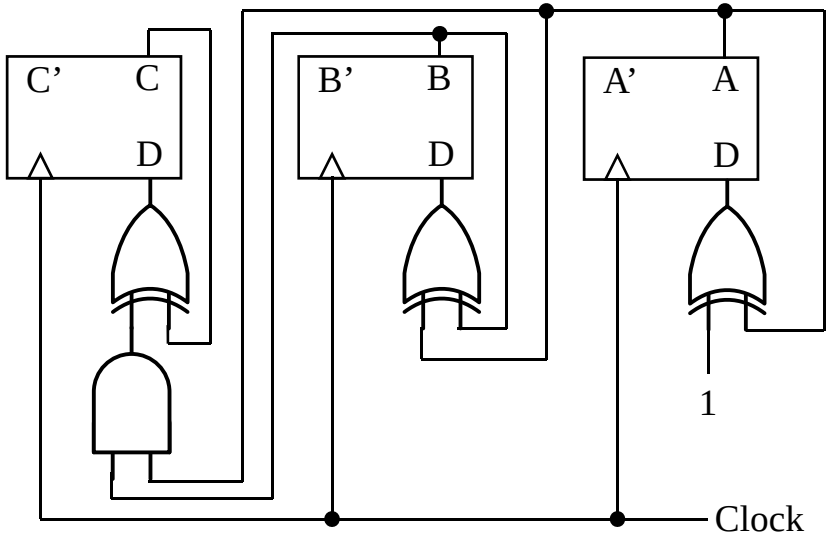
With D F/F

Tips: Q+ = D

C	B	A	C^+	B^+	A^+	D_C	D_B	D_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0



$D_C = C \oplus BA$ $D_B = B \oplus A$ $D_A = A'$

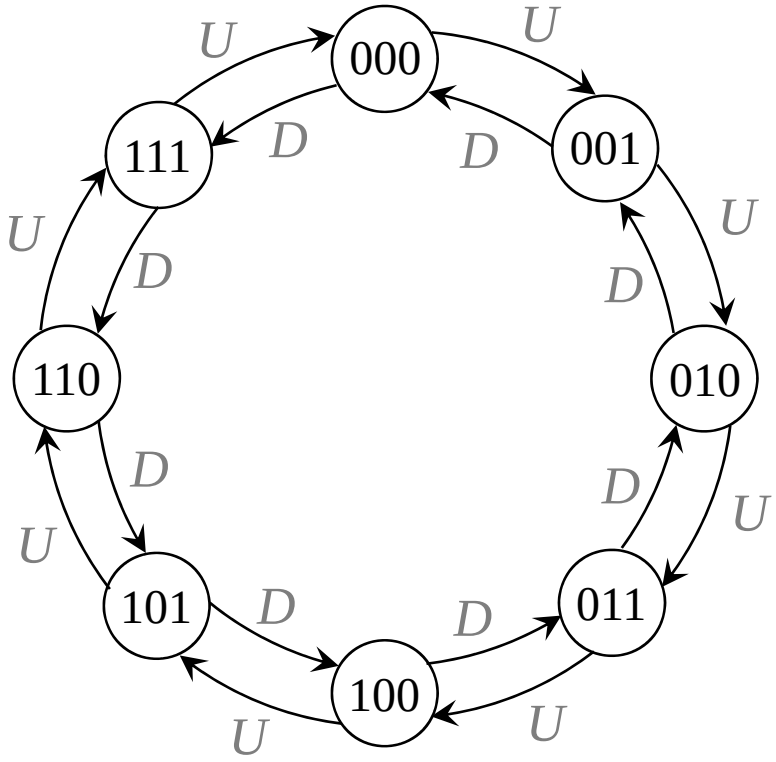


Design of a Binary Counter (6/11)

Up-down counter

U = 1 *D = 1*

State graph



(U, D) = (1, 0) Up
= (0, 1) Down
= (0, 0) intact
= (1, 1) not allowed

C	B	A	C^+	B^+	A^+	C^+	B^+	A^+
0	0	0	0	0	1	1	1	1
0	0	1	0	1	0	0	0	0
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	0	1	0
1	0	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0	0
1	1	0	1	1	1	1	0	1
1	1	1	0	0	0	1	1	0

$D_A = A \oplus (U+D)$

$D_B = B \oplus (UA+DA')$

$D_C = C \oplus (UBA+DB'A')$

Design of a Binary Counter (7/11)

- U = 1 and D = 0 (up counter)

$D_A = A^+ = A'$

$D_B = B^+ = BA' + B'A = B \oplus A$

$D_C = C^+ = C'BA + CB' + CA' = C'BA + C(BA)' = C \oplus BA$

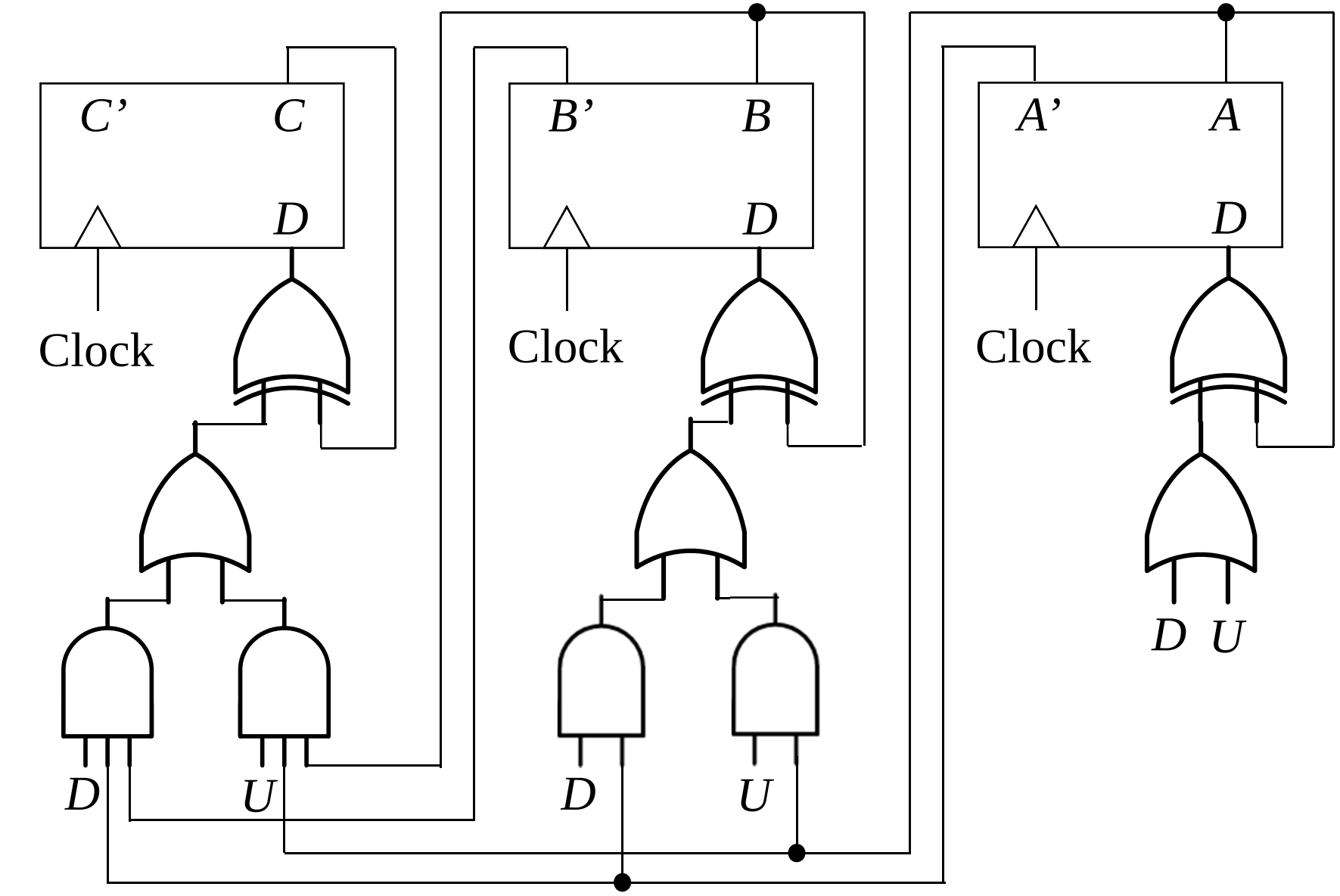
- U = 0 and D = 1 (down counter)

$D_A = A^+ = A \oplus 1 = A'$ **(A changes state every clock cycle)**

$D_B = B^+ = B \oplus A'$ **(B changes state when A = 0)**

$D_C = C^+ = C \oplus B'A'$ **(C changes state when B = A = 0)**

Design of a Binary Counter (8/11)

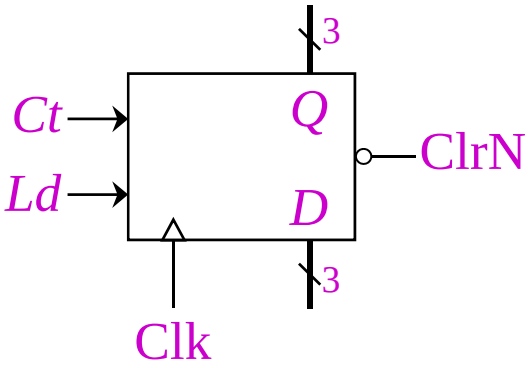


Design of a Binary Counter (9/11)

Loadable Counter with Count Enable

- Two control signals *Ld* (load) and *Ct* (count) and an asynchronous clear *ClrN*
  - *Ld=1, Ct=0* binary data is loaded into counter
  - *Ld=0, Ct=1* the counter is incremented
  - *Ld=0, Ct=0* the counter holds its present state
  - *Ld=1, Ct=1* load overrides count, data is loaded into the counter
  - *ClrN=0,* clears the counter
  - State changes on the rising clock edge

Design of a Binary Counter (10/11)



(a)

ClrN	*Ld*	*Ct*	C^+	B^+	A^+	
0	×	×	0	0	0	
1	1	×	D_C	D_B	D_A	(load)
1	0	0	C	B	A	(no change)
1	0	1	Present state + 1			

(b)

- **Next-state Equations**

$$A^+ = D_A = (Ld' \cdot A + Ld \cdot D_{Ain}) \oplus Ld' \cdot Ct$$

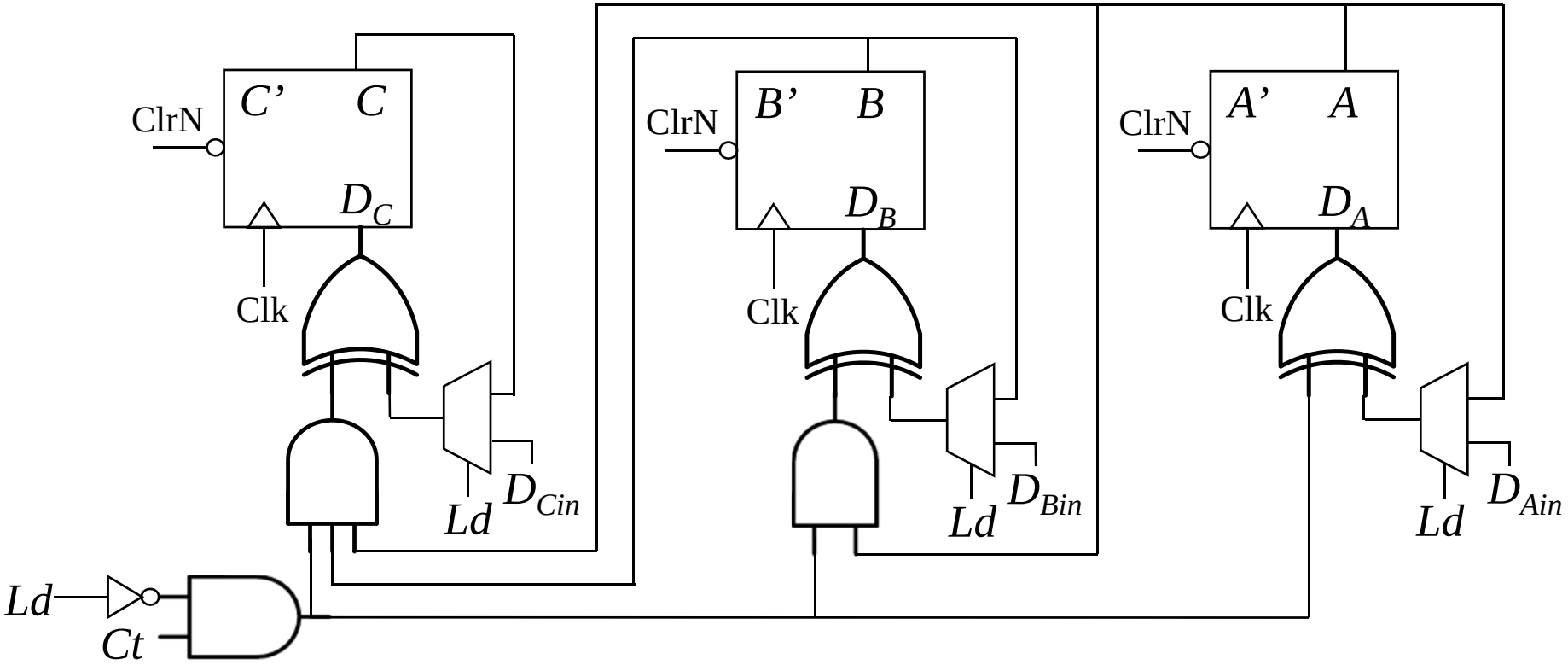
$$B^+ = D_B = (Ld' \cdot B + Ld \cdot D_{Bin}) \oplus Ld' \cdot Ct \cdot A$$

$$C^+ = D_C = (Ld' \cdot C + Ld \cdot D_{Cin}) \oplus Ld' \cdot Ct \cdot B \cdot A$$

Mux

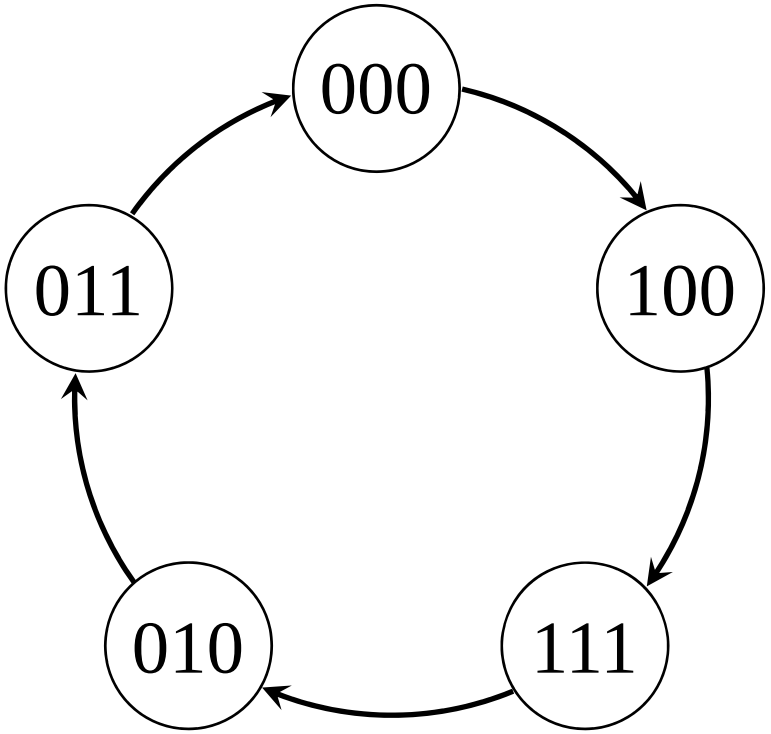
Design of a Binary Counter (11/11)

- **Implementation using F/Fs, MUXes, and gates**



Counters for Other Sequences (1/9)

- **Example:** Design a counter which counts in the sequence : 000,100,111,010,011 using **T F/Fs** and gate



C	B	A	C^+	B^+	A^+
0	0	0	1	0	0
0	0	1	–	–	–
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	–	–	–
1	1	0	–	–	–
1	1	1	0	1	0

Counters for Other Sequences (2/9)

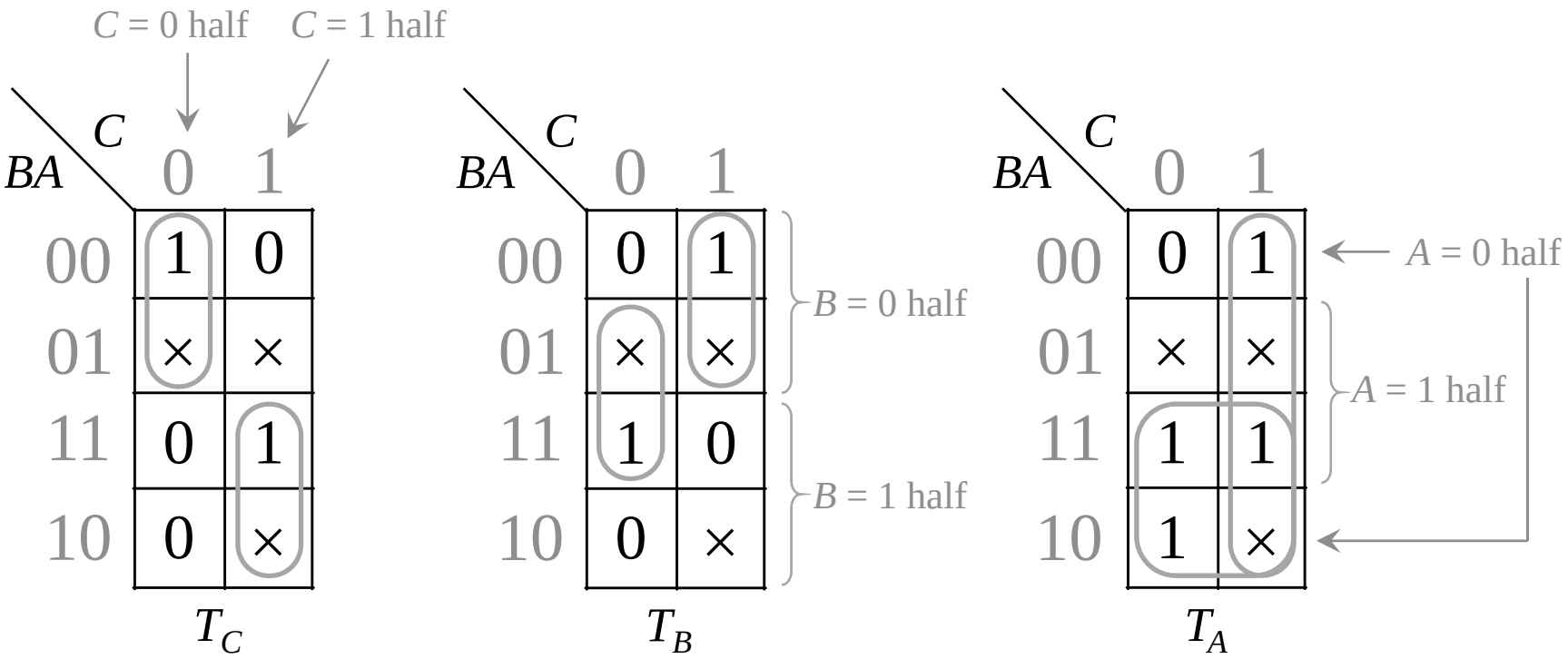
- **Sol** : The T F/F application table:

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

$$T = Q^+ \oplus Q$$

C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	1	0	0	1	0	0
0	0	1	–	–	–	–	–	–
0	1	0	0	1	1	0	0	1
0	1	1	0	0	0	0	1	1
1	0	0	1	1	1	0	1	1
1	0	1	–	–	–	–	–	–
1	1	0	–	–	–	–	–	–
1	1	1	0	1	0	1	0	1

Counters for Other Sequences (3/9)



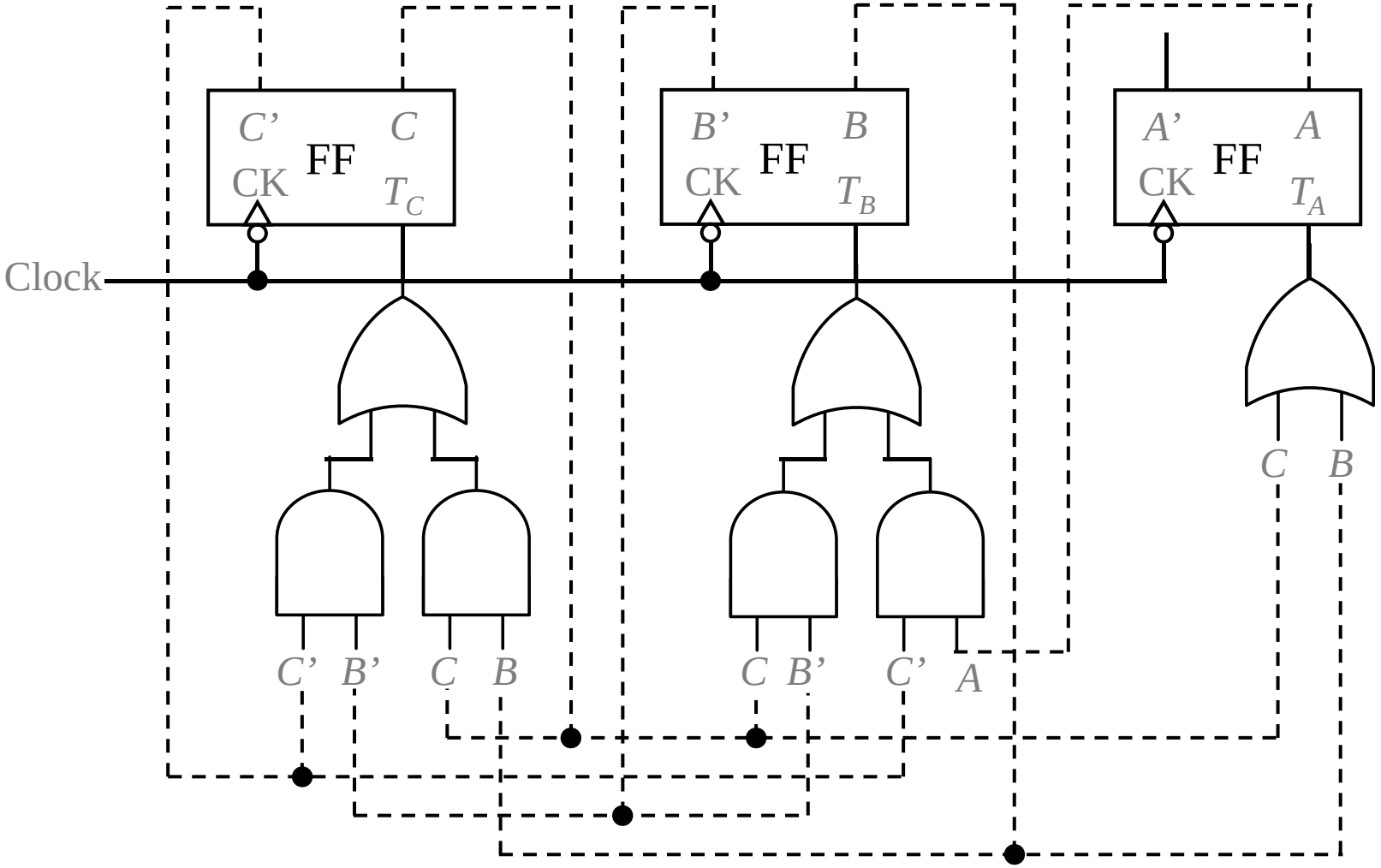
$T_C = C'B' + CB$

$T_B = C'A + CB'$

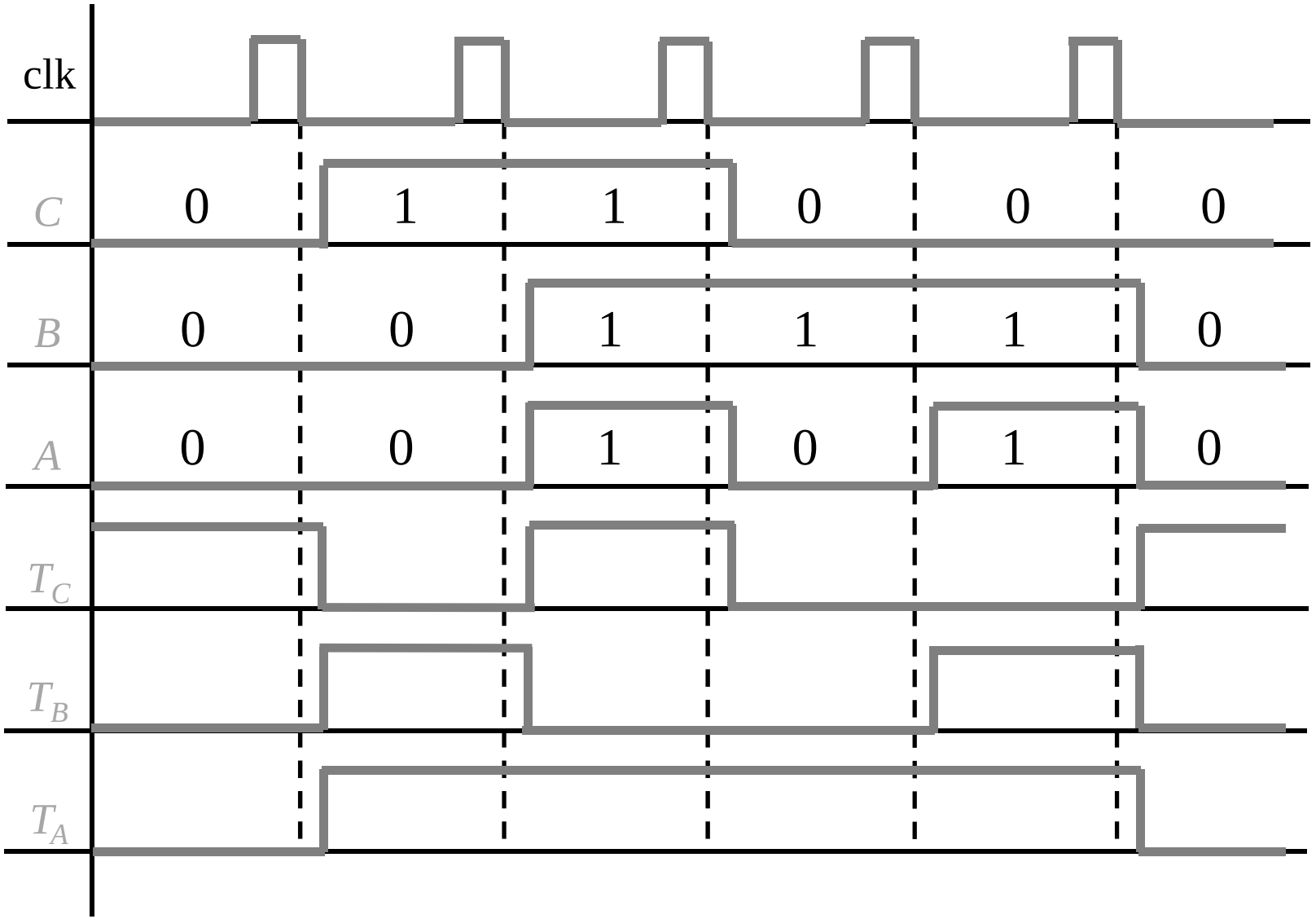
$T_A = C + B$

Derivation of T inputs

Counters for Other Sequences (4/9)



Counters for Other Sequences (5/9)

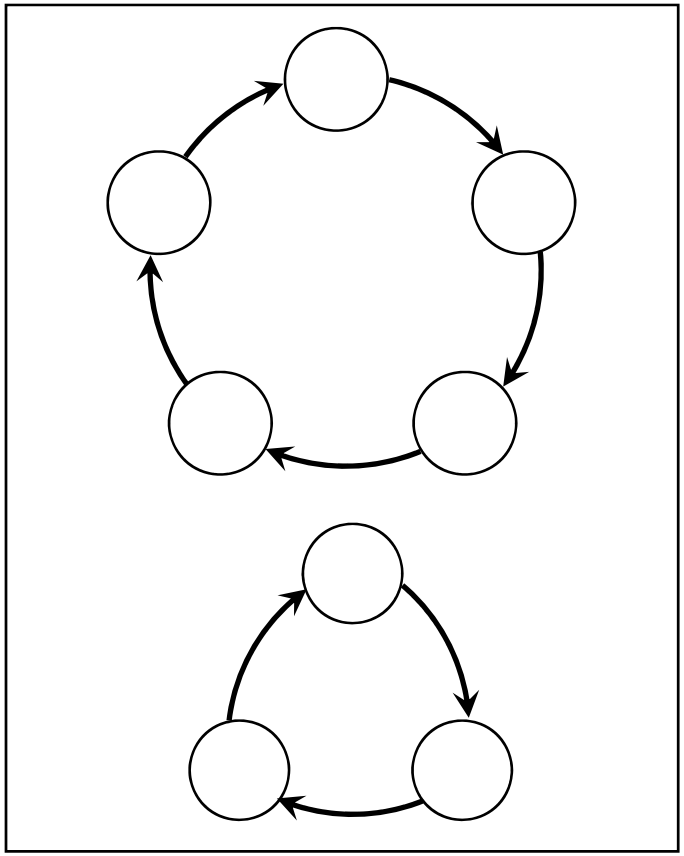


Counters for Other Sequences (6/9)

- **Summary**
  - When the power in a circuit is first turned on, the initial states of the Flip-Flops *may be unpredictable*. All of the don't care states in a counter should be checked to make sure that they eventually lead into the main counting sequence
  - Don't care states : 001, 110, 101
    - 001: T_C=C'B'+CB=0'·0'+0·0=1,
      T_B=C'A+CB'=0'·1+0·0'=1,
      T_A=C+B=0+0=0. 001➔111
    - 110: ($T_C T_B T_A$)=(101) 110➔011
    - 101: ($T_C T_B T_A$)=(011) 101➔110 ➔011

Counters for Other Sequences (7/9)

Must enter the
main counting loop



Counters for Other Sequences (8/9)

- **Example:** Design the same sequence counter using **D F/Fs**

C	B	A	C^+	B^+	A^+	D_C	D_B	D_A
0	0	0	1	0	0	1	0	0
0	0	1	–	–	–	X	X	X
0	1	0	0	1	1	0	1	1
0	1	1	0	0	0	0	0	0
1	0	0	1	1	1	1	1	1
1	0	1	–	–	–	X	X	X
1	1	0	–	–	–	X	X	X
1	1	1	0	1	0	0	1	0

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

D F/F excitation table

Q+=D

$D_C = C+ = B'$;

$D_B = B+ = C+BA'$;

$D_A = A+ = CA'+BA'$

$= A'(C+B)$

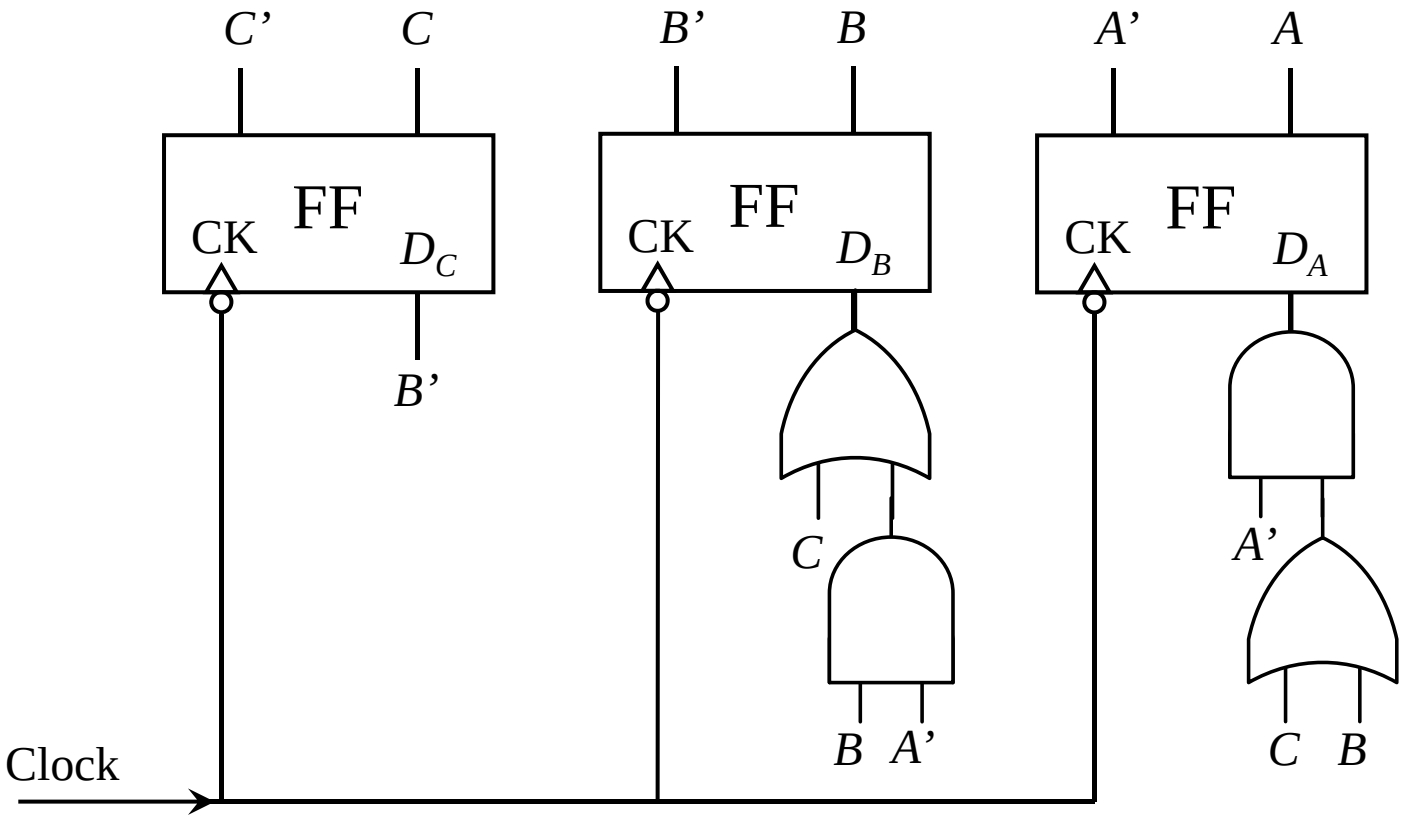
Counters for Other Sequences (9/9)

Q+=D

$D_C = C+ = B'$;

$D_B = B+ = C + BA'$;

$D_A = A+ = CA' + BA' = A'(C+B)$



Counters Design Using S-R F/Fs (1/3)

- **Example:** Design the same sequence counter using **S-R F/Fs** and gate

C	B	A	C^+	B^+	A^+
0	0	0	1	0	0
0	0	1	–	–	–
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	–	–	–
1	1	0	–	–	–
1	1	1	0	1	0

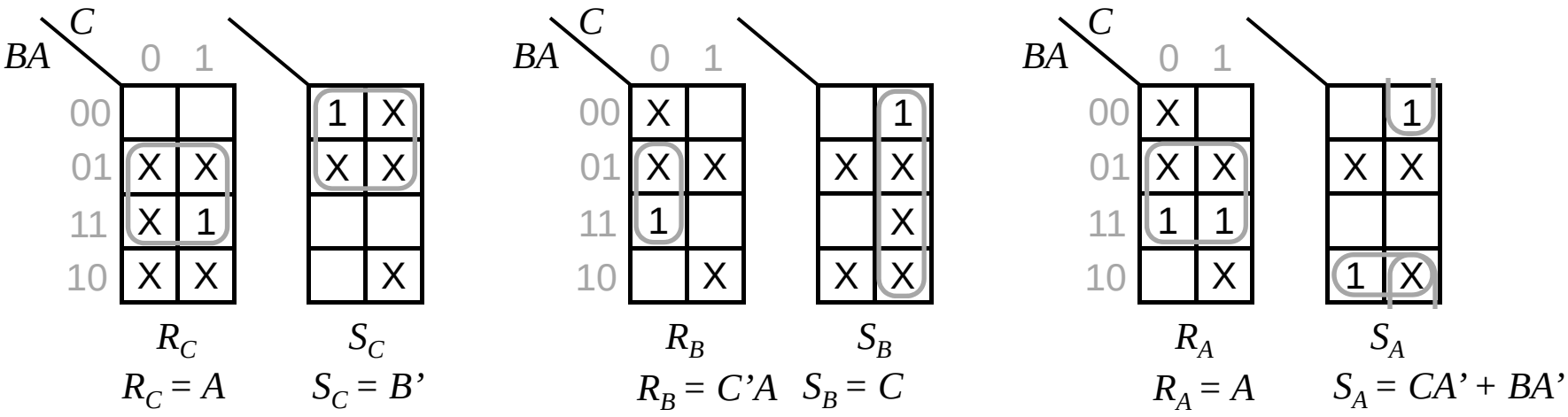
Q	Q^+	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Counters Design Using S-R F/Fs (2/3)

Present State			Next State			Required S-R Inputs					
C	B	A	C^+	B^+	A^+	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	1	0	0	1	0	0	×	0	×
0	0	1	–	–	–	×	×	×	×	×	×
0	1	0	0	1	1	0	×	×	0	1	0
0	1	1	0	0	0	0	×	0	1	0	1
1	0	0	1	1	1	×	0	1	0	1	0
1	0	1	–	–	–	×	×	×	×	×	×
1	1	0	–	–	–	×	×	×	×	×	×
1	1	1	0	1	0	0	1	×	0	0	1

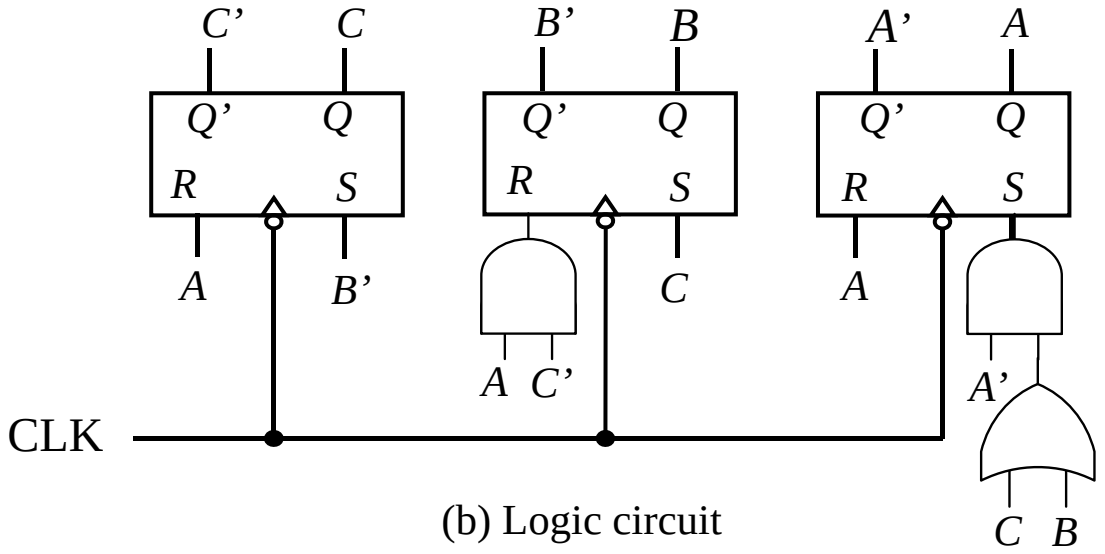
Q	Q^+	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Counters Design Using S-R F/Fs (3/3)



$R_C = A$ $S_C = B'$ $R_B = C'A$ $S_B = C$ $R_A = A$ $S_A = CA' + BA' = A'(C + B)$

(a) S-R flip-flop equations



(b) Logic circuit

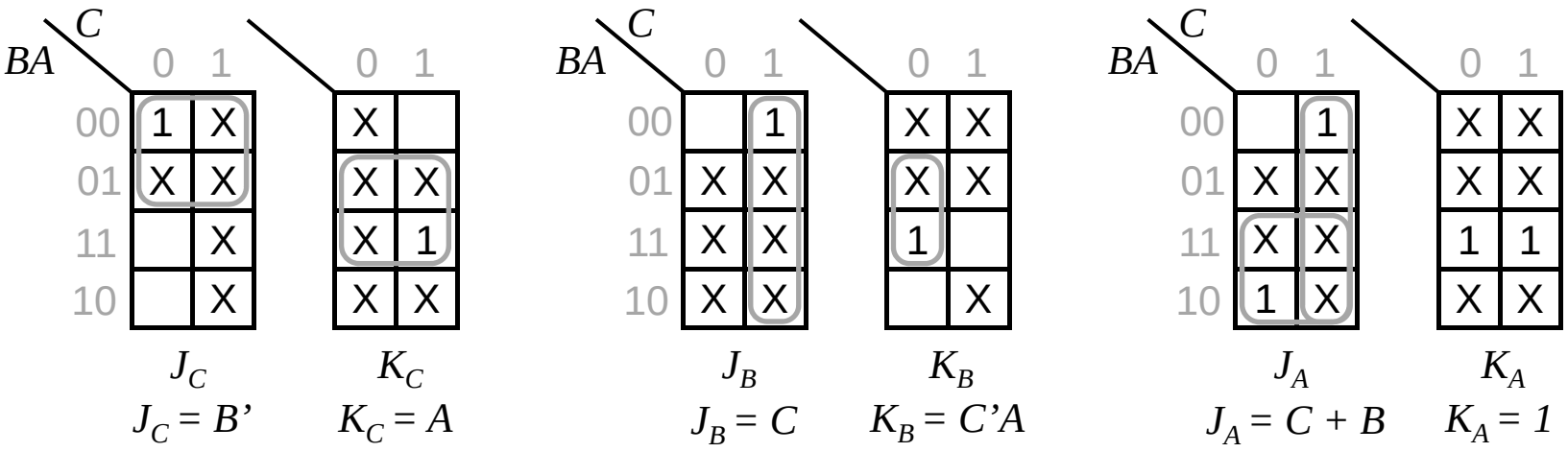
Counters Design Using J-K F/Fs (1/2)

- **Example:** Design the same sequence counter using **J-K F/Fs** and gate

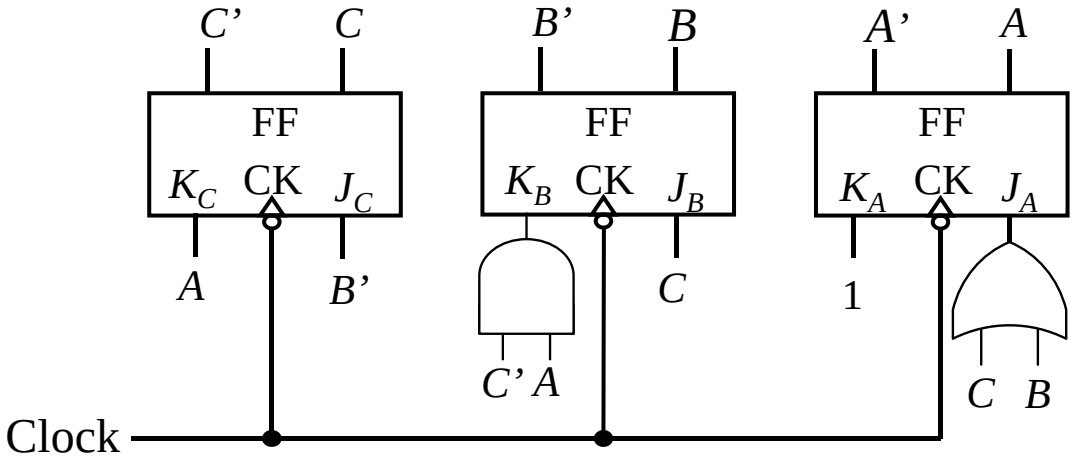
C	B	A	C^+	B^+	A^+	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	1	0	0	1	×	0	×	0	×
0	0	1	–	–	–	×	×	×	×	×	×
0	1	0	0	1	1	0	×	×	0	1	×
0	1	1	0	0	0	0	×	×	1	×	1
1	0	0	1	1	1	×	0	1	×	1	×
1	0	1	–	–	–	×	×	×	×	×	×
1	1	0	–	–	–	×	×	×	×	×	×
1	1	1	0	1	0	×	1	×	0	×	1

Q	Q^+	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Counters Design Using J-K F/Fs (2/2)



(a) J-K flip-flop input equations



(b) Logic circuit (omitting the feedback lines)

Flip-Flop Application Tables (1/5)

- **Characteristic equations**
  - **S-R F/F** : $Q^+=S+R'Q$ $(S \cdot R=0)$
  - **D F/F** : $Q^+=D$
  - **J-K F/F** : $Q^+=JQ'+K'Q$
  - **T F/F** : $Q^+=TQ'+T'Q$

- **Derivation of F/F Application Tables**

Example: For S-R F/F,

Q=0, Q+=0, 0=S+R'0, ==> S=0, R=don't care (SR=**0**0, SR=**0**1)

Q=0, Q+=1, 1=S+R'0, ==> S=1, R=0 (S·R=0)

Q=1, Q+=0, 0=S+R'1, ==> S=0, R=1

Q=1, Q+=1, 1=S+R'1, ==> S=don't care, R=0 (SR=1**0**, SR=0**0**)

Flip-Flop Application Tables (2/5)

- **D Flip-Flop**

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

$$Q^+ = D$$

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

- **T Flip-Flop**

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

$$Q^+ = T'Q + TQ' = T \oplus Q$$

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Flip-Flop Application Tables (3/5)

- **S-R Flip-Flop**

(a)

S	R	Q	Q^+	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	–	inputs not allowed
1	1	1	–	

(b)

Q	Q^+	S	R
0	0	0	0
		0	1
0	1	1	0
1	0	0	1
1	1	0	0
		1	0

(c)

Q	Q^+	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Flip-Flop Application Tables (4/5)

- **J-K Flip-Flop**

(a)

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b)

Q	Q^+	J	K
0	0	0	0
		0	1
0	1	1	0
		1	1
1	0	0	1
		1	1
1	1	0	0
		1	0

(c)

Q	Q^+	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Flip-Flop Application Tables (5/5)

Q	Q^+	S	R
0	0	0	--
0	1	1	0
1	0	0	1
1	1	--	0

S-R F/F

Q	Q^+	J	K
0	0	0	--
0	1	1	--
1	0	--	1
1	1	--	0

J-K F/F

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

D F/F

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

T F/F